AN3309
Application note

Clock configuration tool for STM32L1xx microcontrollers

Introduction

This application note presents the clock system configuration tool for the STM32L1xx microcontroller family.

This purpose of this tool is to help user configure the microcontroller clocks, taking into consideration the product parameters (power supply, product voltage range, the Flash access mode...).

The configuration tool is implemented in the “STM32L1xx_Clock_Configuration_VX.Y.Z.xls” file which is supplied with this application note and can be downloaded from www.st.com.

It makes it easy to take care of all the following system aspects and interdependencies:

- Configure the system clock, HCLK source and output frequency.
- Configure the Core voltage range (V_{CORE}).
- Configure the Flash latency (number of wait states depending on the HCLK frequency).
- Set the PCLK1, PCLK2 and TIMCLK (timer clocks) frequencies.
- Generate a ready-to-use *system_stm32l1xx.c* file with all the above settings (STM32L15x CMSIS Cortex-M3 Device Peripheral Access Layer System Source File).

Note: 1 The STM32L1xx_Clock_Configuration_VX.Y.Z.xls is referred to as “Clock tool” throughout this document.

2 Before using the Clock tool, it is essential to read the STM32L microcontroller reference manual (RM0038). This application note is not a substitute for the reference manual.

Contents

1 Glossary

Table 1. Definition of terms

Term	Description
HCLK	AHB clock
PCLK1	APB1 clock
PCLK2	APB2 clock
TIMCLK	Timer clock
USBCLK	USB clock
ADCCLK	ADC clock
F_{CPU}	Cortex-M3 clock
V_{CORE}	Regulator output voltage
V_{DD}	Power supply
HSI	High speed internal clock
HSE	High speed external clock
MSI	Multi-Speed internal clock

2 Getting started

This section describes the requirements and procedures needed to start using the Clock tool.

2.1 Software requirements

In order to use the Clock tool with Windows operating system, a recent version of Windows, such as Windows XP, Vista or Windows7 must be installed on the PC with at least 256 MB of RAM.

Before starting to use the Clock tool, make sure that Microsoft Office is installed on your machine and then follow these steps:

- Download the latest version of the **Clock tool** available from the ST website www.st.com.
- Enable macros and ActiveX controls:

Excel 1997-2003 version:

a) Click **Tools** in the menu bar
b) Click **Macro**
c) Click **Security**
d) Click **Low (not recommended)**

Note: If ActiveX controls are not enabled, a warning message is displayed asking you to enable ActiveX, in this case you should click "OK" to enable it.

Excel 2007 version:

a) Click the **Microsoft Office** Button, and then click **Excel options**.
b) Click **Trust Center**, click **Trust center settings**, and then click **Macro settings**.
c) Click **Enable all macros (not recommended, potentially dangerous code can run)**.
d) Click **Trust Center**, click **Trust center settings**, and then click **ActiveX settings**.
e) Click **Enable all controls without restrictions and without prompting (not recommended; potentiality dangerous controls can run).**
f) Click **OK**.

Note: For more information about how to enable macros and ActiveX controls please refer to the Microsoft Office website.

2.2 Hardware requirements

2.2.1 Introduction

The Clock tool is designed to configure the system clocks and generate the *system_stm32l1xx.c* file for STM32L1xx (Ultra low power microcontrollers).

The *system_stm32l1xx.c* file is provided as a template system clock configuration file which can be easily modified to select the corresponding system clock frequency, the V_{CORE} and also to configure the Flash latency.

2.2.2 Clock scheme for STM32L1xx microcontrollers

This section describes the system clock scheme, the voltage requirements (V_{DD} and V_{CORE}) versus the system clock frequency.

Four different clock sources can be used to drive the system clock (SYSCLK):

- **HSI** (16 MHz) oscillator clock.
- **HSE** oscillator clock.
- **PLL** clock.
- **MSI** (65 KHz,131 KHz, 262 KHz, 524 KHz, 1 MHz, 2 MHz, 4 MHz**)** oscillator clock
  MSI Range 0 = 65.536 kHz.
  MSI Range 1 = 131.072 kHz.
  MSI Range 2 = 262.144 kHz.
  MSI Range 3 = 524.288 kHz.
  MSI Range 4 = 1048 kHz.
  MSI Range 5 = 2097 kHz.
  MSI Range 6 = 4194 kHz.

Figure 1. Clock scheme for STM32L1xx medium-density

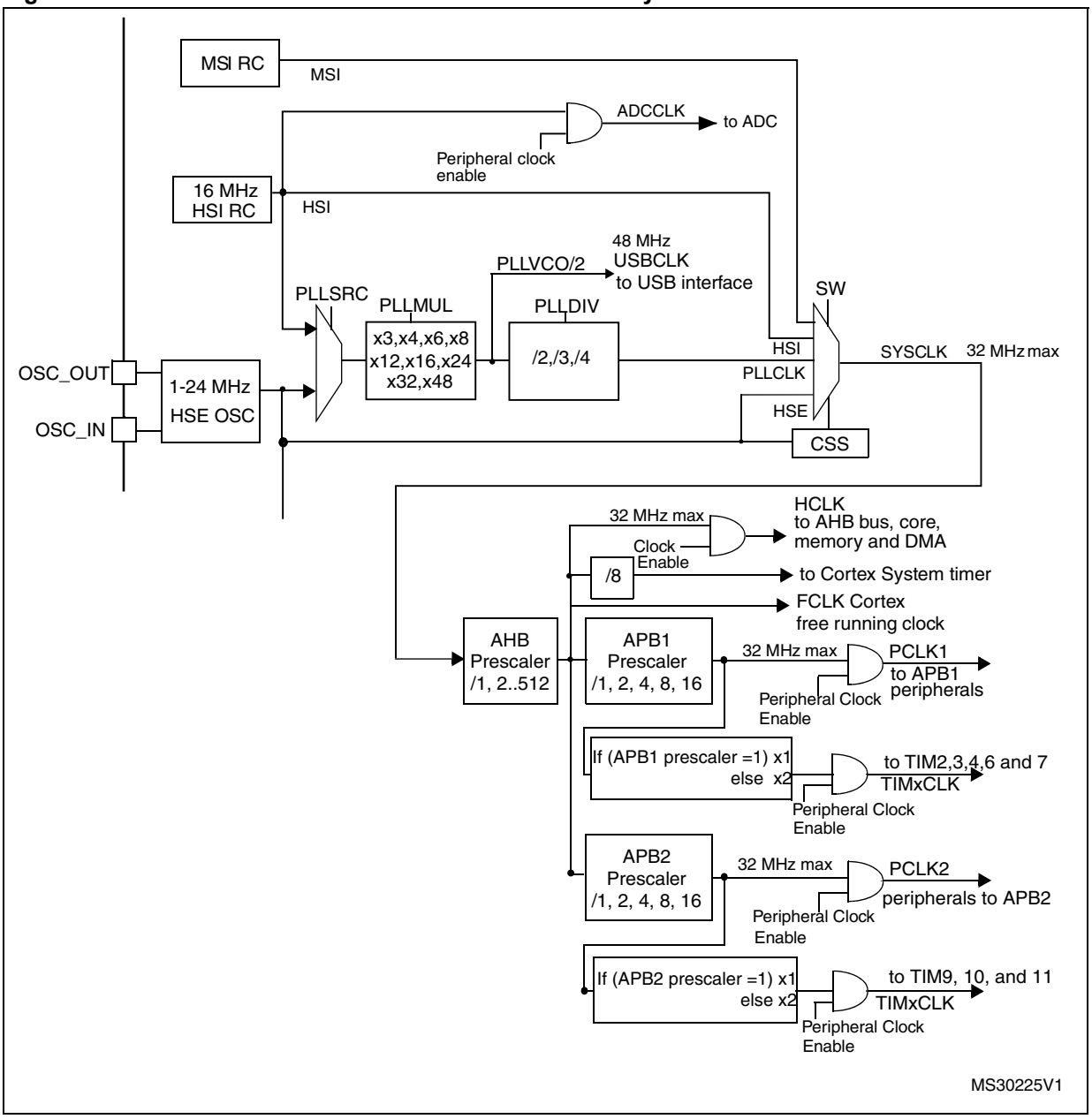
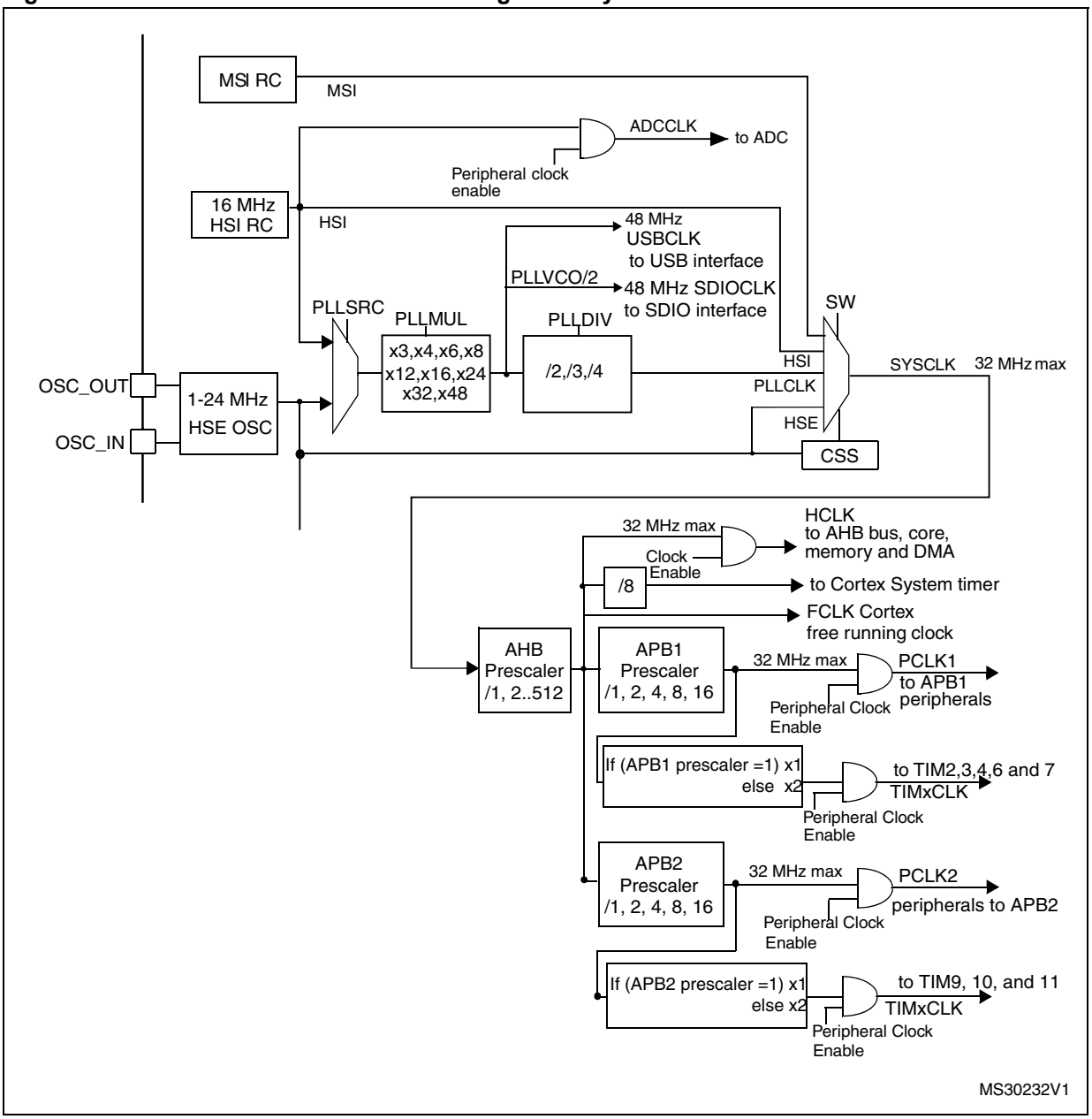


Figure 2. Clock scheme for STM32L1xx high-density



System clock source frequency versus V_{CORE}

All the system clock sources depend on the V_{CORE} voltage range:

- **MSI**: this clock source can be used with all the V_{CORE} ranges (1.2 V, 1.5 V and 1.8 V (only when V_{DD} > 2 V)).
- **HSI**: the HSI clock cannot be used when V_{CORE} = 1.2 V (Range 3).
- **HSE**: the HSE clock frequency can range from 1 MHz (2 MHz when it is used as the PLL input clock) to 24 MHz using crystal oscillator (32 MHz using the external clock). The frequency must be chosen in accordance with the selected V_{CORE} range. The maximum HSE frequency is:

  - 24 MHz when the V_{CORE} = 1.8 V (Range 1)

  - 16 MHz when the V_{CORE} = 1.5 V (Range 2)

  - 4 MHz when the V_{CORE} = 1.2 V (Range 3)
- **PLL**: the PLLVCO (defined by the PLL multiplication factor) also depends on the V_{CORE} value since its maximum value is:

  - 96 MHz when V_{CORE} = 1.8 V (Range 1)

  - 48 MHz when V_{CORE} = 1.5 V (Range 2)

  - 24 MHz when V_{CORE} = 1.2 V (Range 3)

  When using PLL as system clock source the input clock frequency must be between 2 MHz and 24 MHz.

  If the USB interface is used in the application, the PLLVCO must be programmed to output a 96 MHz frequency. This is required to provide a 48 MHz clock to the USB interface since the USBCLK is equal to PLLVCO divided by 2. For accuracy reasons, the USB peripheral must only be driven by the PLL configured with the HSE clock source.

Note: When V_{CORE} Range 3 (V_{CORE} = 1.2 V) is selected, the ADC peripheral can only operate at low speed sampling frequency (ADCCLK = 4 MHz, 250 ksps) and the ADC prescaler must be set to 4.

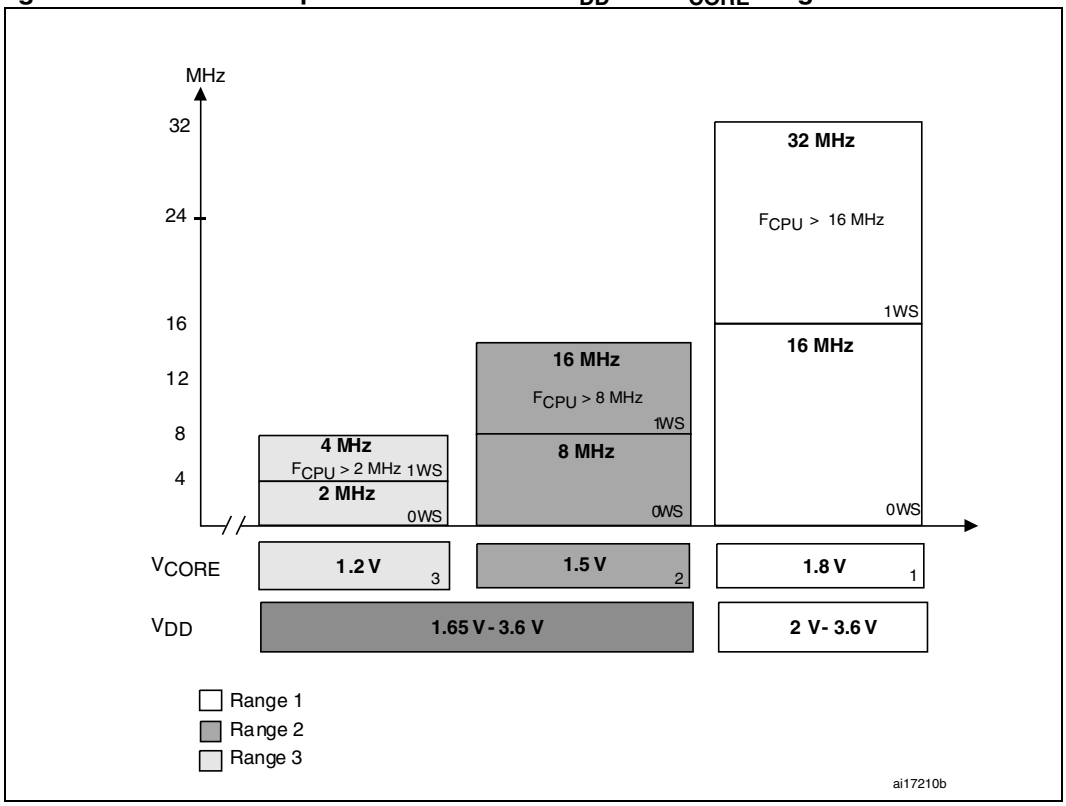
STM32L1xx performance versus V_{DD} and V_{CORE} range

The number of Flash memory wait states (latency) is defined according to the frequency of the CPU (Cortex-M3) and indirectly by the supply voltage of the device (V_{DD}):

- If V_{CORE} = 1.8 V (Range 1):
  - 0 Flash wait states are required when the CPU frequency is less than or equal to 16 MHz
  - 1 Flash wait state is required when the CPU frequency is greater than 16 MHz
- If V_{CORE} = 1.5 V (Range 2)
  - 0 Flash wait states are required when the CPU frequency is less than or equal to 8MHz
  - 1 Flash wait state is required when the CPU frequency is greater than 8 MHz
- If V_{CORE} = 1.2 V (Range 3)
  - 0 Flash wait states are required when the CPU frequency is less than or equal to 2 MHz
  - 1 Flash wait state is required when the CPU frequency is higher than 2 MHz

Refer to *Figure 3: STM32L1xx performance versus V_{DD} and V_{CORE} range on page 9* for a description of the STM32L1xx operating conditions versus the V_{CORE}.

Figure 3. STM32L1xx performance versus V_{DD} and V_{CORE} range

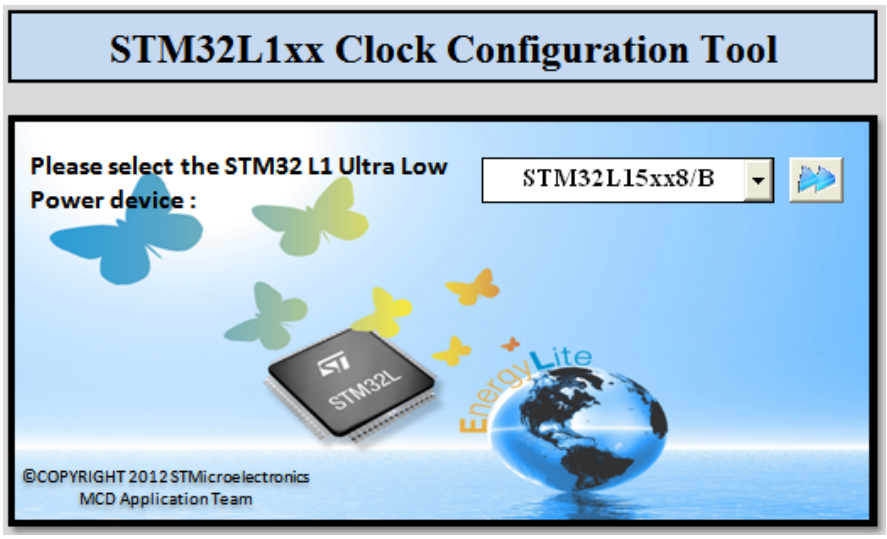


3 Tutorials

This section describes step by step how to use the Clock tool to configure all the system clocks and generate the *system_stm32l1xx.c* file.

Before starting with this tool, the user should select the device as show in the following figure.

Figure 4. Device selection menu



The Clock tool is designed to configure the system clocks for the following devices:

1. Ultra low power medium-density devices (STM32L151xx and STM32L152xx) where the Flash memory density ranges between 64 and 128 Kbytes.
2. Ultra low power medium-density-plus devices (STM32L151xx, STM32L152xx and STM32L162xx) where the Flash memory density is 256 Kbytes.
3. Ultra low power high-density devices (STM32L151xx, STM32L152xx and STM32L162xx) where the Flash memory density is 384 Kbytes.

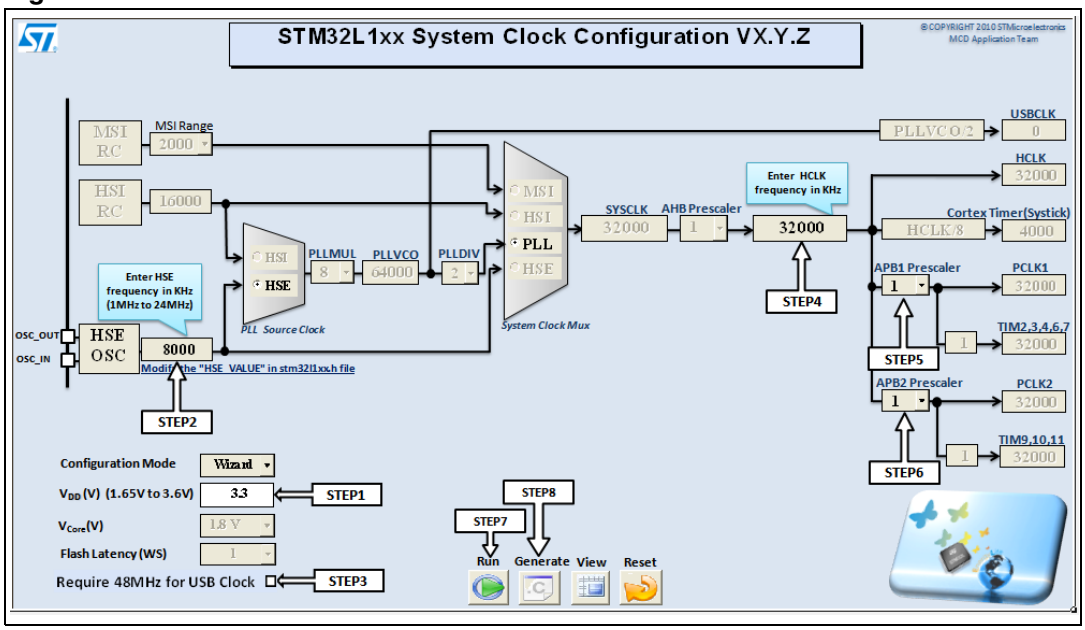
The next sections are based on the STM32L15xx8/B microcontrollers.

Two modes are available: **Wizard** and **Expert**. The selection is made in the **Configuration mode** list box.

3.1 Wizard mode

This mode (default mode) guides you through a series of steps to obtain the desired clock system configuration quickly and easily.

Figure 5. Wizard mode user interface



*Note: 1 The **View** button is used to activate or deactivate viewing the xls file in full screen mode.*

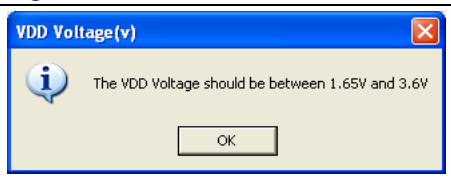
*2 The **Reset** button is used to set the system clock to the default configuration:*

- *MSI (Range 5) as system clock source*
- *V_{DD} = 3.3 V*
- *V_{CORE} = 1.5 V*
- *Flash Latency (WS) = 0*
- *HCLK = 2000 KHz*
- *AHB, APB1 and APB2 prescalers are set to 1*
- *HSE Clock value is 8 MHz*

Step-by-step procedure:

1. Enter the V_{DD} power supply voltage range between 1.65 V and 3. V. Refer to *Figure 5: Wizard mode user interface*). If the V_{DD} voltage is out of range, an error message will be displayed as shown in *Figure 6*.

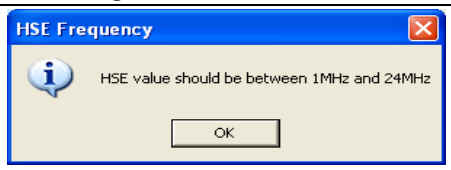
Figure 6. V_{DD} out of range



2. If the HSE is used in your application, set its frequency between:
   - A minimum of 1 MHz or 2 MHz if is used as the PLL input clock
   - A maximum of 24 MHz if a crystal oscillator is used.

   If the frequency you entered is out of range, an error message is displayed, as shown in *Figure 7*. You then have to enter a valid frequency.

Figure 7. HSE value out of range

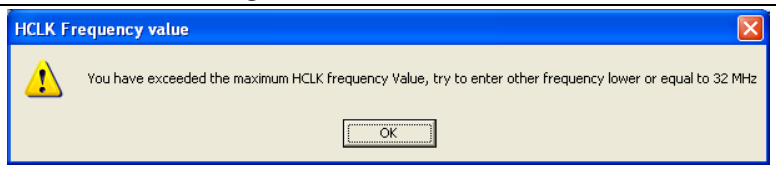


3. Specify if a 48 MHz clock is needed for USB operation. If yes, this will add a constraint to the parameter setting in the PLL configuration. The USB can be used only when V_{CORE} is equal to 1.8 V and V_{DD} is equal to at least 2 V.
4. Set the HCLK (AHB clock) frequency in KHz. The maximum frequency of HCLK depends on V_{CORE} and also the Flash latency, and must be less than 32 MHz.

   In this Clock Tool, the following MSI values are used:
   - 65 KHz instead of 65536 Hz
   - 131 KHz instead of 131072 Hz
   - 262 KHz instead of 262144 Hz
   - 524 KHz instead of 524288 Hz
   - 1000 KHz instead of 1048 KHz
   - 2000 KHz instead of 2097 KHz
   - 4000 KHz instead of 4191 KHz

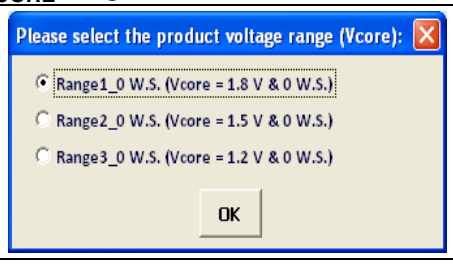
   If the entered value is higher than 32 MHz an error message will be displayed as shown in *Figure 8*.

Figure 8. HCLK error message



5. Select the APB1 prescaler settings from the list box to obtain the desired PCLK1 frequency. The timer clock (TIMCLK) frequencies are configured automatically depending on the APB1 prescaler settings.
6. Select the APB2 prescaler settings from the list box to obtain the desired PCLK2 frequency. The timer clock (TIMCLK) frequencies are configured automatically depending on the APB2 prescaler settings.
7. Click on the **RUN** button.
   – A message box is then displayed requesting you to select the V_{CORE} value and the number of wait states (the selection list depends on the desired HCLK frequency)

Figure 9. Define the V_{CORE} range and the number of Flash wait states

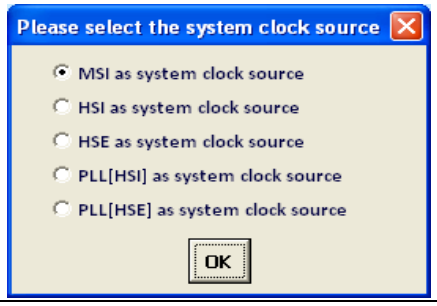


Note: When V_{CORE} Range 3 (V_{CORE} = 1.2 V) is selected, the ADC can only operate at low speed sampling frequency (ADCCLK = 4 MHz, 250 ksps) and the ADC prescaler must be set to 4.

– Check if the requirements you defined above can be achieved.

If yes, a message box is displayed, requesting you to select the clock source as shown in *Figure 10*. You can choose HSE, MSI, HSI or PLL (sourced by HSI or HSE).

Figure 10. Select the clock source



Otherwise, a selection error message is displayed indicating if there is a conflicting requirement. You then have to change the requirements to resolve the conflict.

Figure 11. Selection error

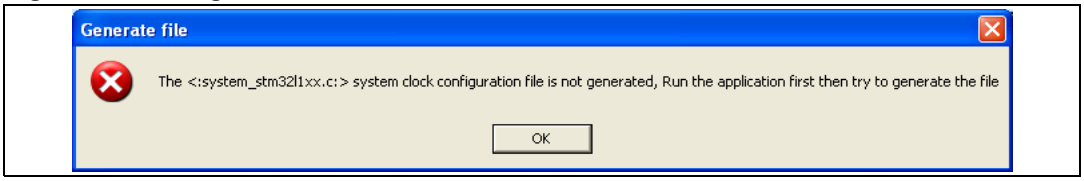
8. Finally, click on the **Generate** button to generate the *system_stm32l1xx.c* file automatically.

   The *system_stm32l1xx.c* is generated in the same location as the Clock tool. You can display the file to verify the value of the system clock *SystemCoreClock* and also the value of AHB, APB1, APB2, the Flash access mode, V_{CORE} and other parameters which are defined in the *SetSysClock* function.

   The *system_stm32l1xx.c* file must be added to the working project to be built.

   If the file is not generated, an error message is displayed as shown in *Figure 12*.

Figure 12. File generation error

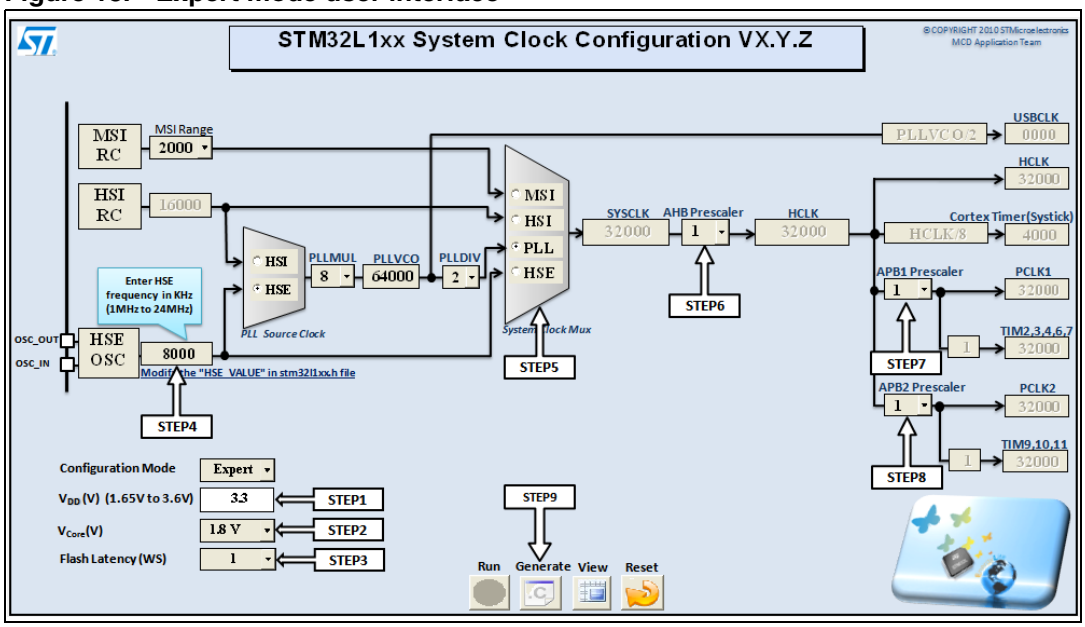


3.2 Expert mode

This mode provides more flexibility in the configuration but it is up to the user to ensure the configuration correctness.

Several steps should be followed *Figure 13: Expert mode user interface*:

Figure 13. Expert mode user interface



*Note: 1 The **View** button is used to activate or deactivate viewing the xls file in full screen mode.*

*2 The **Reset** button is used to set the system clock to the default configuration:*

- *MSI (Range 5) as system clock source*
- *V_{DD} = 3.3 V*
- *V_{CORE} = 1.5 V*
- *Flash Latency (WS) = 0*
- *HCLK = 2000 KHz*
- *AHB, APB1 and APB2 prescalers are set to 1*
- *HSE Clock value is 8 MHz*

Step-by-step procedure

1. Enter the V_{DD} power supply voltage range between 1.65 V and 3.6 V. Refer to *Figure 13: Expert mode user interface*).
2. Set the V_{CORE} to 1.2 V, 1.5 V or 1.8 V (depending on the V_{DD} value).

Note: When V_{DD} < 2 V, Range 1 (V_{CORE} = 1.8V) is not available.

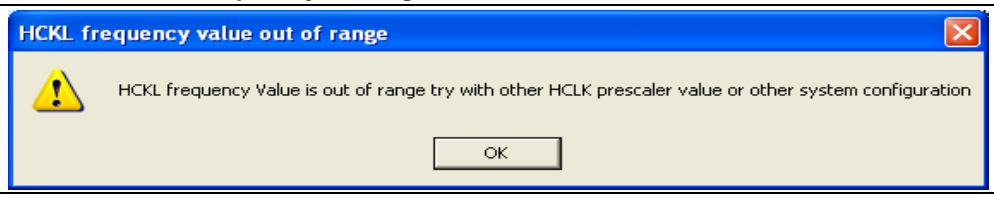
When V_{CORE} = 1.2 V (Range 3), the ADC can only operate at low speed sampling frequency (ADCCLK = 4 MHz, 250 cusps) and the ADC prescaler should be set to 4.

3. Configure the Flash memory latency from the **Flash wait state** list box.
4. If the HSE is used in your application, set its frequency between:
   - A minimum of 1 MHz or 2 MHz if it is used as the PLL input clock
   - A maximum of frequency which is determined by the V_{CORE} range previously selected in step 2 above.

   If the frequency you entered is out of range, the Clock Tool automatically restores the last correct HSE clock value.
   - With V_{CORE} = 1.2 V (Range 3) the maximum HSE frequency is 4 MHz
   - With V_{CORE} = 1.5 V (Range 2), the maximum HSE frequency is 16 MHz
   - with V_{CORE} = 1.8 V (Range 1), the maximum HSE frequency is 24 MHz
5. Configure the System clock source (PLL, MSI, HSE or HSI). If you select PLL as System clock source you also have to select the source clock for the PLL (HSE or HSI).

   If the clock source selection is invalid (the HCLK frequency is too high) an error message is displayed as shown in *Figure 14*.

Figure 14. HCLK frequency too high



6. Configure the AHB prescaler using the **AHB Prescaler** list box to obtain the desired HCLK frequency.

If the HCLK frequency is too high, an error message as shown in *Figure 14*.

7. Select the APB1 prescaler settings from the list box to obtain the desired PCLK1 frequency. The timer clock (TIMCLK) frequencies are configured automatically depending on the APB1 prescaler settings.
8. Select the APB2 prescaler settings from the list box to obtain the desired PCLK2 frequency. The timer clock (TIMCLK) frequencies are configured automatically depending on the APB2 prescaler settings.
9. Finally, click on the **Generate** button to generate the *system_stm32l1xx.c* file automatically.

   The *system_stm32l1xx.c* file is generated in the same location as the Clock tool. You can display the file to verify the value of the system clock “SystemCoreClock” and also the value of AHB, APB1, APB2, the Flash access mode, $V_{CORE}$and other parameters which are defined in the “SetSysClock” function.

The *system_stm32l1xx.c* file must be added to the working project to be built.

4 Known limitations

This sections describes the known limitations of the system clock configuration tool (Clock tool):

- This tool does not support configurations that use HSE external clock source.
- This tool does not support the fractional value of the HSE.

5 Conclusion

This application note provides a description of how to use the Clock tool for the STM32L1xx microcontroller devices. Using either one of the two configuration modes, this tool generates a source code file *system_stm32l1xx.c* to configure the clock system of the STM32L.

Wizard mode is the first mode and provides a quick and easy way to configure the system clocks.

Expert mode is the second mode. It gives you more flexibility in setting up the system clock configuration while still respecting all the product constraints.

6 Revision history

Table 2. Document revision history

Date	Revision	Changes
03-Jan-2011	1	Initial release.
26-Jan-2012	2	Updated *Figure 1: Clock scheme for STM32L1xx medium-density* Added *Figure 2: Clock scheme for STM32L1xx high-density* Added *Figure 4: Device selection menu*