



AN3114

Application note

How to use
the STM8L15x LCD controller

Introduction

This application note describes techniques for connecting the STM8L15x LCD controller to liquid crystal displays (LCD), for driving alphanumeric characters and converting ASCII characters to LCD segment control codes.

It explains how to select the LCD glass well suited for your application, and how to configure the LCD controller to take into account key parameters such as contrast, power consumption, number of used pixels, operating frequency range, and blinking.

A brief description of the LCD segment drive firmware embedded on the STM8L1526-EVAL evaluation board is also provided.

For more information on the STM8L15x LCD controller, refer to the STM8L15x reference manual (RM0031).

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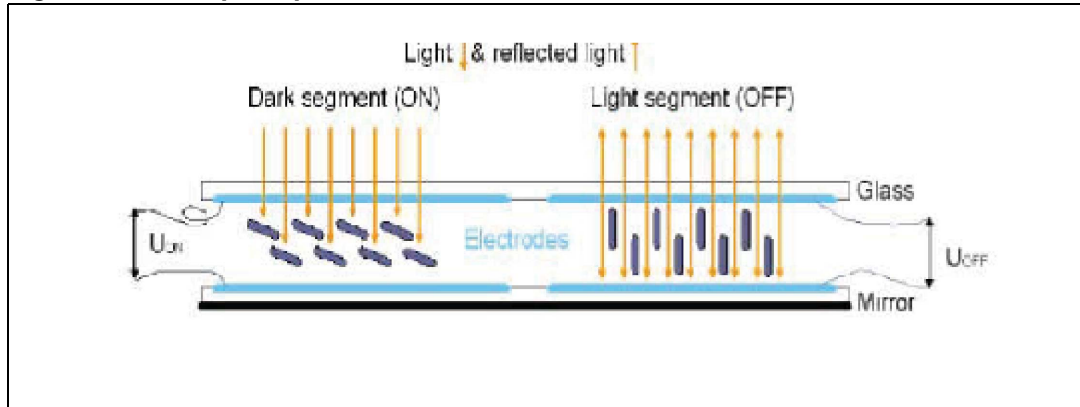
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1 LCD solution

1.1 LCD principle

Figure 1. LCD principle



An LCD panel is composed of many layers. A liquid crystal is filled between two of them (glass plates), that are separated by thin spacers coated with transparent electrodes which contain orientation layers.

The orientation layer usually consists of a polymer (e.g. polyimide) which has been unidirectionally rubbed using, for instance, a soft tissue. As a result, the liquid crystal molecules are fixed with their alignment more or less parallel to the plates, in the direction of rubbing. The crystal alignment directions at the surface of the two plates are perpendicular so that the molecules between the two plates undergo a homogeneous twist deformation in alignment to form a helix.

If no electric field is applied, the birefringent liquid crystal molecules keep their helical structure and rotate linearly polarized light waves passing through the plates. The transmitted light wave is then allowed through a crossed exit polarizer. As a result, the modulator has a bright appearance. On the other hand, if an AC voltage of a few volts is applied, the resulting electric field forces the liquid crystal molecules to align themselves along the field direction and the twist deformation (the helix) is unwound. In this case, the polarization of the incident light is not rotated by the crystal molecules and the crossed exit polarizer blocks the light wave. As a result, the modulator appears dark.

The inverse switching behavior can be obtained with parallel polarizers. It must also be noted that gray scale modulation is easily achieved by varying the voltage between the crystal molecule reorientation threshold (reorientation is resisted by the elastic properties of liquid crystals) and the saturation field.

LCDs are sensitive to root mean square voltage levels. With a low root mean square voltage applied to it, an LCD is practically transparent (the LCD segment is then inactive or off). To turn an LCD segment on, causing the segment to turn dark (from light gray to opaque black), an LCD RMS voltage greater than the LCD threshold voltage is applied to the LCD. The LCD RMS voltage is the RMS voltage across the capacitor C in [Figure 2.](#), which is equal to the potential difference between the SEG and COM values.

The LCD threshold voltage depends on the quality of the liquid used in the LCD and the temperature. The optical contrast is defined by the difference in transparency of an LCD segment that is on (dark) and an LCD segment that is off (transparent). The optical contrast

depends on the difference between the RMS voltage on an on segment (V_{ON}) and the RMS voltage on an off segment (V_{OFF}). The higher the difference between $V_{ON(RMS)}$ and $V_{OFF(RMS)}$, the higher the optical contrast. The optical contrast also depends on the level of V_{ON} versus the LCD threshold voltage. If V_{ON} is lower or close to the threshold voltage, the LCD is completely or almost transparent. If V_{OFF} is close or higher than the threshold voltage, the LCD is completely black.

In this document, the contrast, D , is defined as follows:

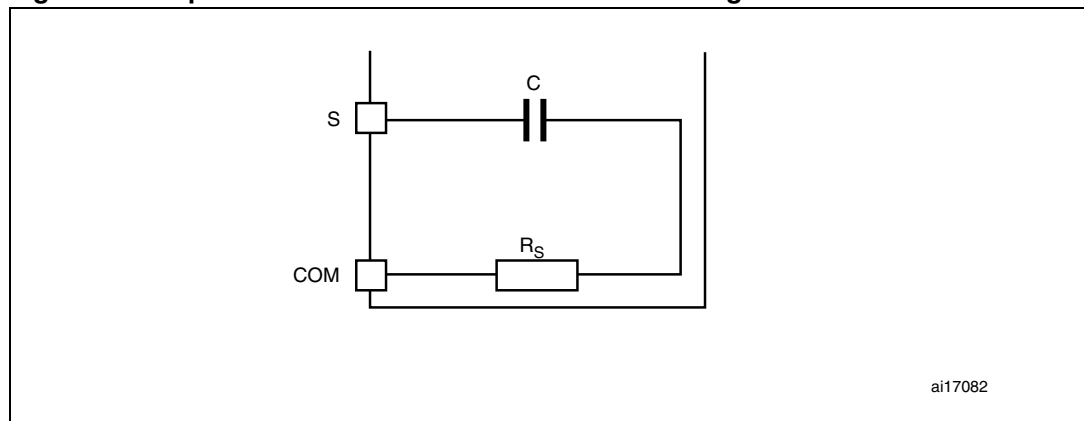
$$D = V_{ON(RMS)} / V_{OFF(RMS)}$$

To prevent the electrolytic process from occurring and consequently ensure a longer LCD lifetime, the applied LCD voltage must also alternate to obtain a zero DC value.

The higher the multiplexing rates, the lower the contrast. The signal period also has to be short enough to avoid visible flickering on the display.

Note: The DC value should never be higher than 100 mV (refer to the LCD manufacturer's datasheet), otherwise, the LCD lifetime may be shortened. The typical frequency ranges from 30 to 100 Hz. If a lower frequency is used, the LCD flickers. If a larger frequency is used, the power consumption increases.

Figure 2. Equivalent electrical schematic of an LCD segment



1.2 Selecting an LCD glass

To select the LCD glass best suited for your application among the wide range of products available on the market, the following criteria must be taken into account:

1. The information to display on the LCD glass. It is a combination of alphanumeric symbols and various useful predefined symbols such as digits, bells, low-battery symbol, arrows, antenna, and progress bar.
2. The typical electrooptical characteristics required for the LCD to operate: operating temperature, storage temperature, and operating voltage, which affect the LCD contrast.
3. The number of pixels required to achieve the desired display on the LCD.

1.3 Typical applications

The STM8L15x LCD controller can be used in many embedded applications. They can be classified as follows:

1. **Home appliances:** refrigerator, microwave oven, coffee maker, washing machine, thermostat, battery management, security system, baby alarm, and clock radio, etc.
2. **Medical:** spirometer, glucose meter, pressure meter, temperature reader, nurse call system, medical pump, and pulse oximeter, etc.
3. **Automotive:** dashboard, audio system, tire pressure sensor, battery vehicle display, iPod adapter, etc.
4. **Industrial:** data acquisition, pressure meter, portable instruments, gasoline pumps, air conditioner, payment systems, gas detection, etc.

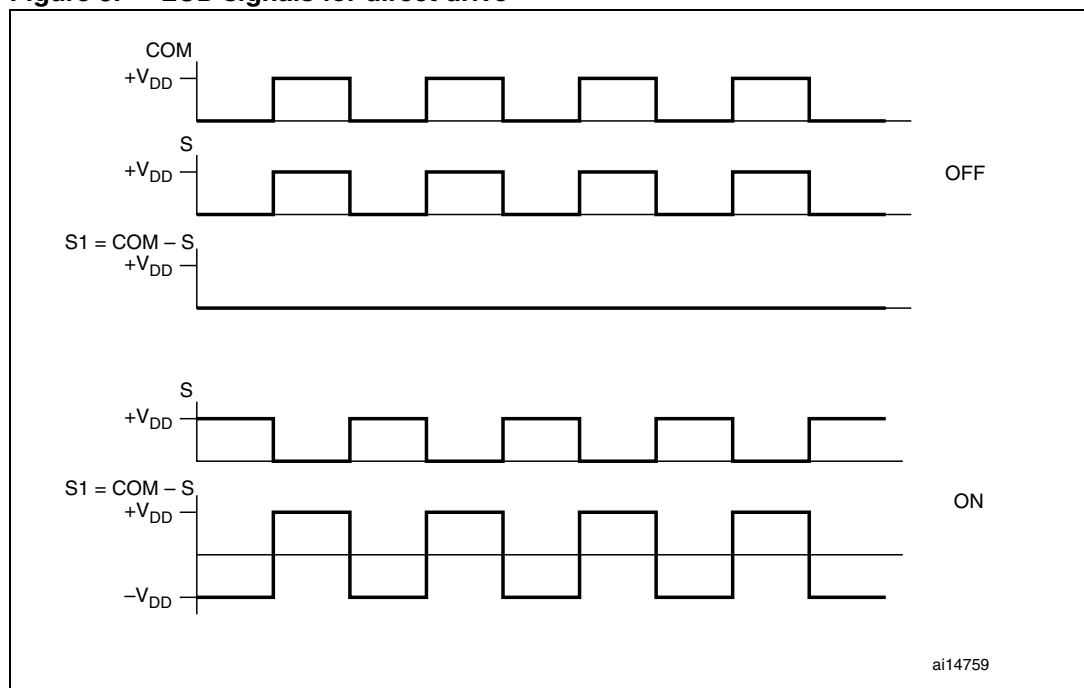
2 LCD controller drive signals

2.1 Single backplane LCD drive

In a single backplane drive, each LCD segment is connected to a segment line (S_x) and to a backplane (common line) common to all the segments. A display using S segments is driven with $S+1$ MCU output lines (S segments + 1 common). The backplane is driven with a COM signal between 0 and V_{DD} with a duty cycle of 50%.

When switching on a segment, a signal with opposite polarity to COM is sent to the corresponding Segment pin. When the non inverted COM signal is sent to the Segment pin, the segment is off. Using an MCU, the I/O operates in output mode at either logic 0 or 1.

Figure 3. LCD signals for direct drive



2.2 Duplex LCD drive

In a duplex drive, two backplanes are used instead of one. Each LCD segment line (S_x) is connected to two LCD segments, which other side is connected to one of the two backplanes or common lines (refer to [Figure 4](#)). Thus, only $(S/2)+2$ MCU pins are necessary to drive an LCD with S segments.

Three different voltage levels have to be generated on the backplanes: 0, $V_{DD}/2$ and V_{DD} . The Segment voltage levels are 0 and V_{DD} only. [Figure 5](#) shows typical backplane, segment and LCD waveforms. The intermediate voltage $V_{DD}/2$ is only required for the backplane voltages. When one backplane is active (0 V), the other is inactive ($V_{DD}/2$).

Figure 4. Basic LCD segment connection in duplex mode

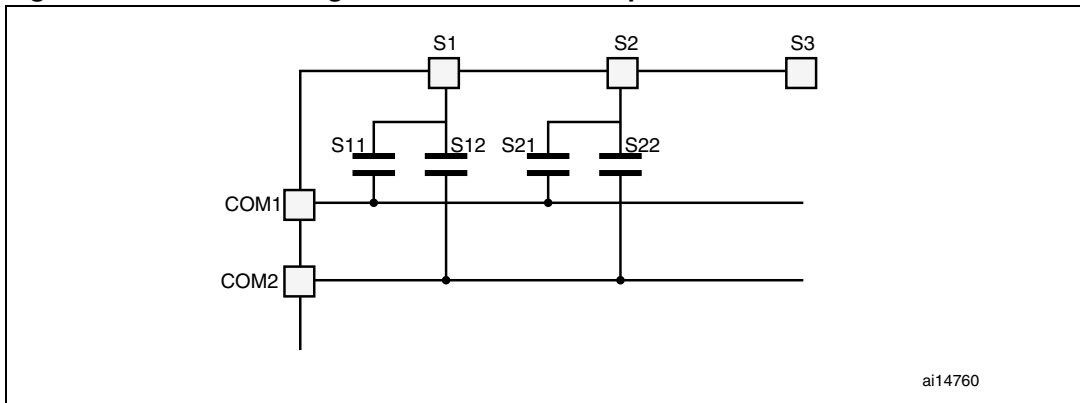
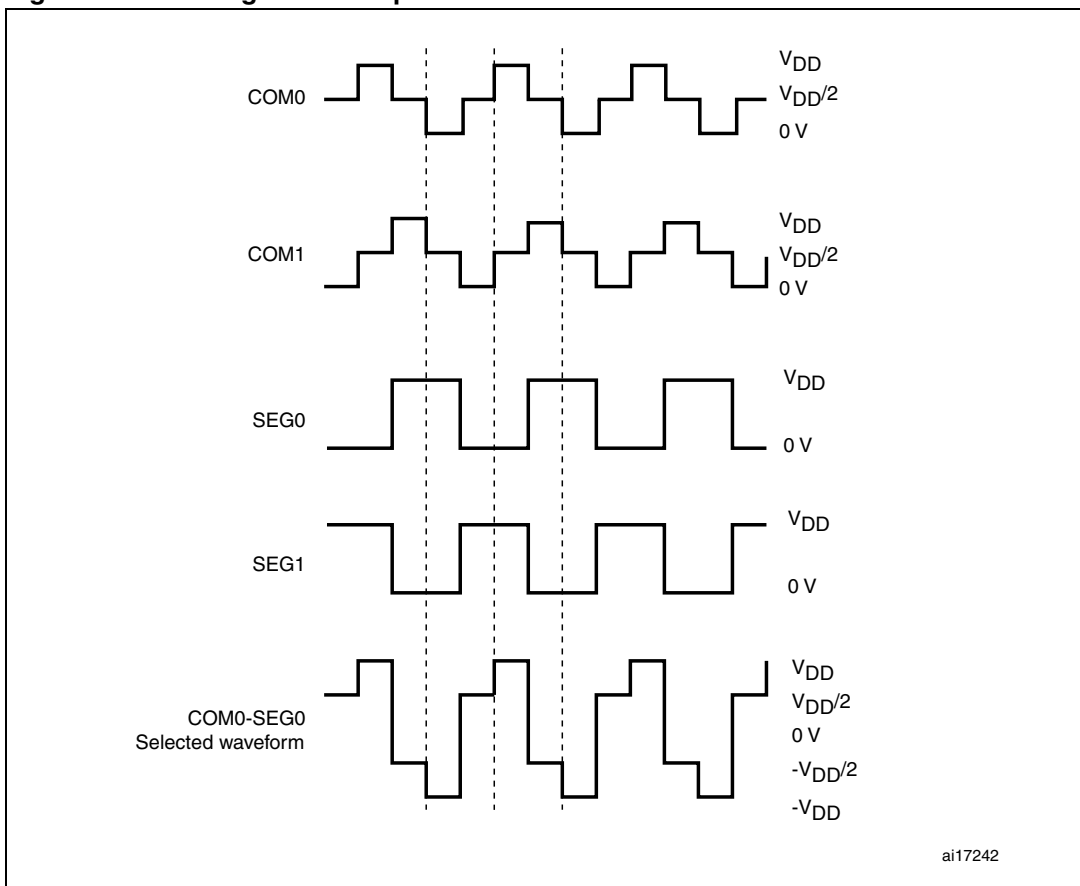


Figure 5. LCD signals for duplex mode



2.3 Quadruplex LCD drive

In a quadruplex LCD drive, four backplanes are used. Each LCD pin is connected to four LCD segments, which other side is connected to one or two of the four backplanes. Consequently, only $(S/4)+4$ MCU pins are necessary to drive an LCD with S segments. For example, to drive an LCD with 112 segments (28 x 4), only 32 I/O ports are required (28 I/O ports to drive the segments and 4 I/O ports to drive the backplanes).

Four different voltage levels have to be generated on the common lines: 0, $V_{DD}/3$, $2V_{DD}/3$ and V_{DD} . The Segment line voltage levels are also 0, $V_{DD}/3$, $2V_{DD}/3$ and V_{DD} . The LCD segment is inactive if the RMS voltage is below the LCD threshold voltage, and is active if the LCD RMS voltage is above the threshold. *Figure 7* shows typical backplane, Segment and LCD waveforms. The intermediate voltage $V_{DD}/3$ and $2V_{DD}/3$ are required for backplane voltages. When a backplane or COM is active (0 V), the others are inactive by applying $2V_{DD}/3$ to them.

Figure 6. Basic LCD segment connection in quadruplex mode

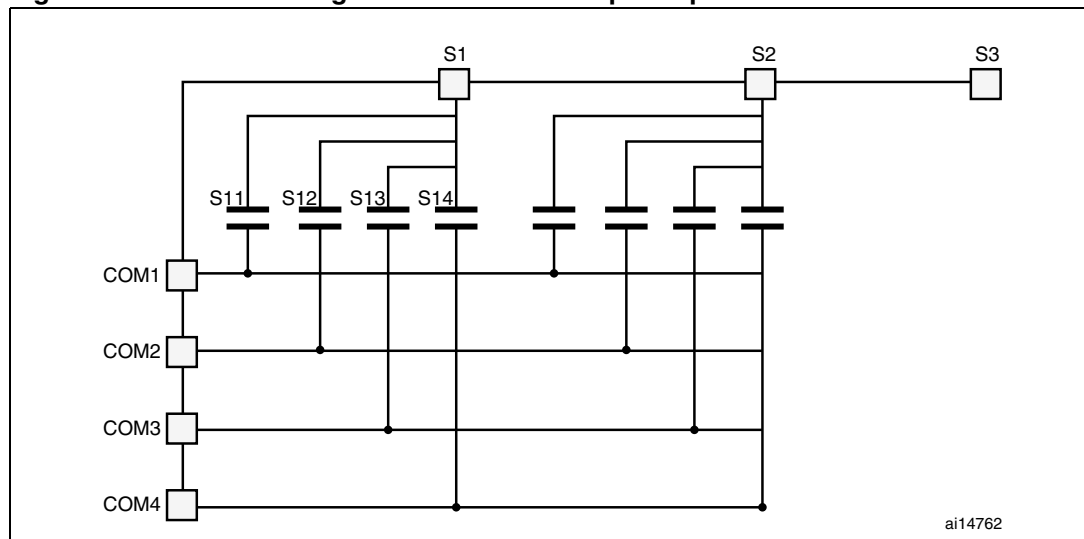
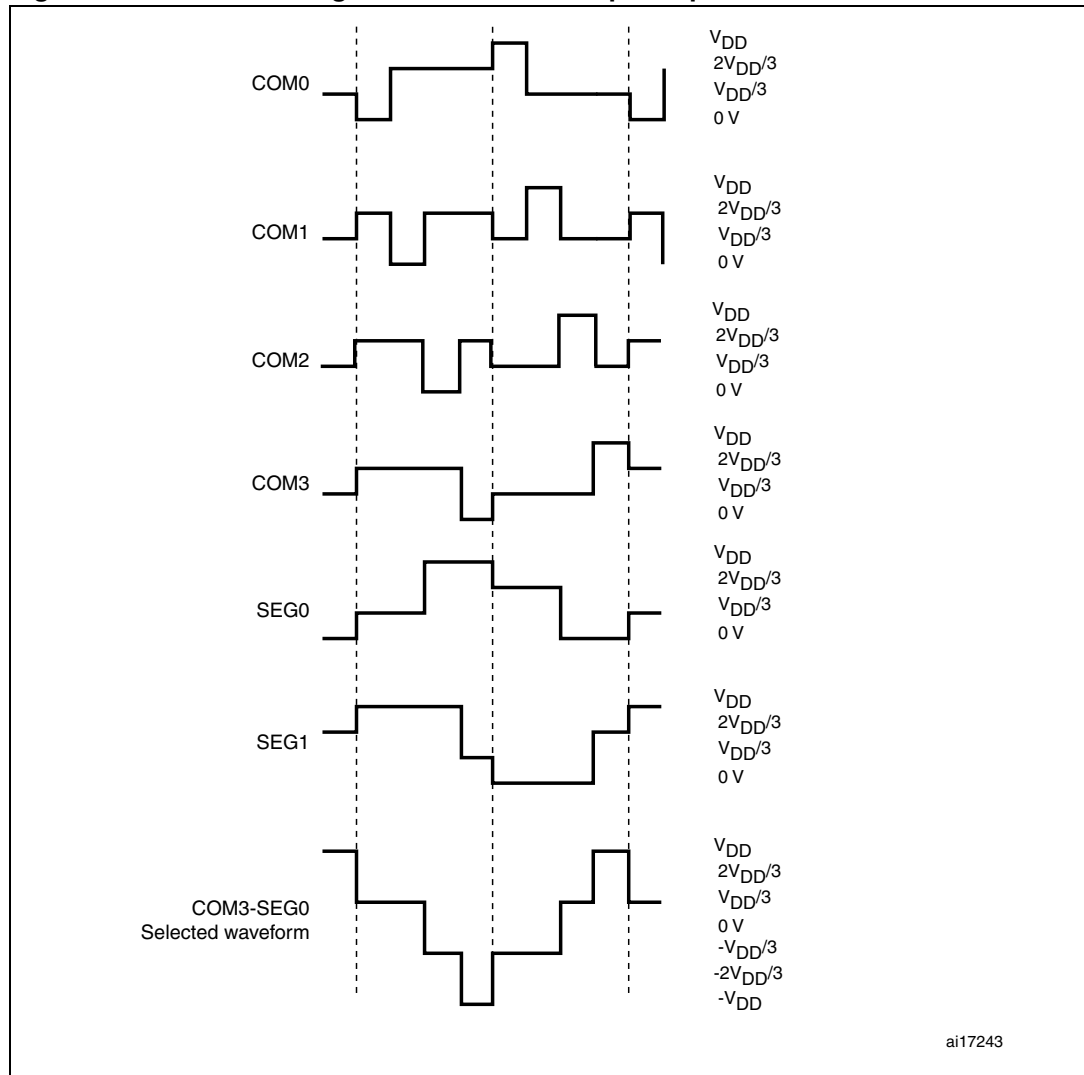


Figure 7. Basic LCD segment connection in quadruplex mode



3 Integrated LCD controller

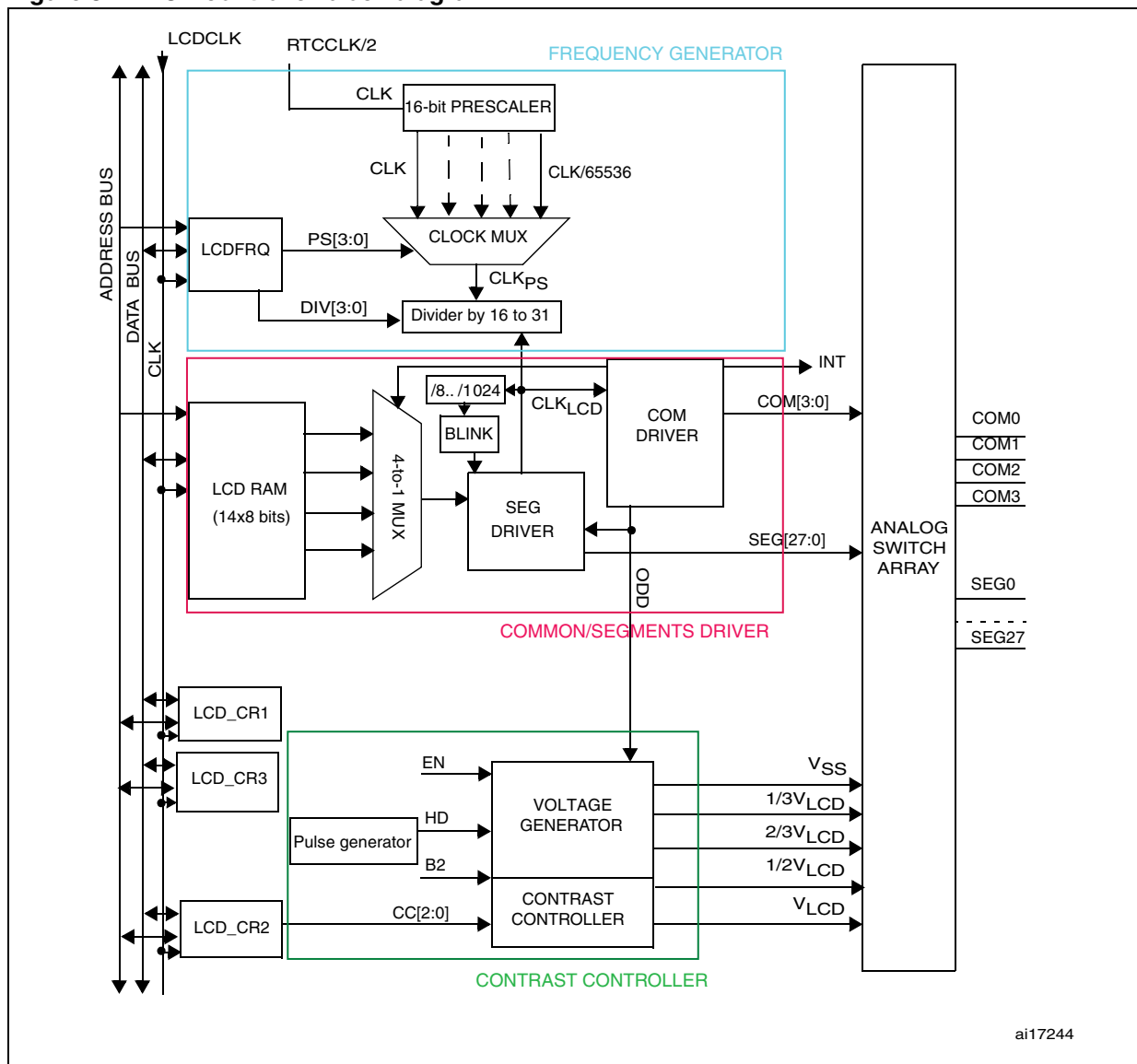
3.1 Benefits of integrated LCD controllers

The STM8L15x integrated LCD control module offers several advantages: its overall design is optimized to achieve an immediate reduction in component count and board space saving, thus reducing the total system cost and power consumption.

The LCD controller is composed of three main blocks (see *Figure 8: LCD controller block diagram*):

- The frequency generator
- The common/segments driver
- The contrast controller

Figure 8. LCD controller block diagram



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3.1.1 Frequency generator block

The first block of the LCD controller is the frequency generator. It consists of a 16-bit ripple counter prescaler and a programmable clock divider with a divider factor ranging from 16 to 31. It generates the LCD frequency, f_{LCD} , starting from the input clock frequency, f_{CLK} . The 16-bit prescaler divides f_{CLK} by 1 up to 65536. The value can be configured through the PS[3:0] bits in the LCD_FRQ register. If a finer resolution rate is required, a second divider can be used to further divide f_{CLK} by a factor of 16 to 31. This second factor is configured through the DIV[3:0] bits in the LCD_FRQ register. f_{LCD} is given by the following equation:

Equation 1

$$f_{\text{LCD}} = \frac{f_{\text{CLK}}}{2^{\text{PS}} \times (16 + \text{DIV})}$$

f_{frame} is the operating frequency. It should be evaluated by taking into account the operating frequency of the LCD device used in application. This range is typically from 30 to 100 Hz. It is a compromise between power consumption and acceptable refresh rate.

To generate f_{frame} in the LCD operating frequency range using the prescaler and the divider, the CLK input clock must be in the range of 16.384 to 500 kHz. For more details, refer to the clock controller section of the STM8L15x reference manual (RM0031). f_{frame} is given by the following equation:

Equation

$$f_{\text{frame}} = f_{\text{LCD}} \times \text{duty}$$

where the duty can be 1/2, 1/3 or 1/4.

3.1.2 Common/segments drive block

The second block of the LCD controller is the common/segments drive. It contains the timing circuitry which allows to generate the appropriate waveforms to drive the common and the segments lines.

This block also contains the LCD_RAM registers which bits corresponds to the individual pixels to be displayed on LCD device.

In addition the common/segments drive block features, a blink prescaler allows to select the blink frequency. This frequency is defined by setting the BLINKF[2:0] bits of the LCD_CR1 register from 0 to 7. Refer to the STM8L15x reference manual (RM0031) for additional details.

3.1.3 LCD contrast controller block

The last block is the contrast controller. It plays a key role in the LCD controller since it allows to adjust the contrast to the optimal value depending on the power consumption and a satisfactory contrast for the application.

The contrast depends on the booster which is used to generate the V_{LCD} voltage. The booster can be internal or external.

External booster

The external booster is selected by setting VSEL bit to '1' in the LCD_CR2 register. When the external booster is used to generate V_{LCD} , the contrast is controlled by varying the dead time (up to 8 phase periods) between each couple of frames where the COM and SEG values are low simultaneously.

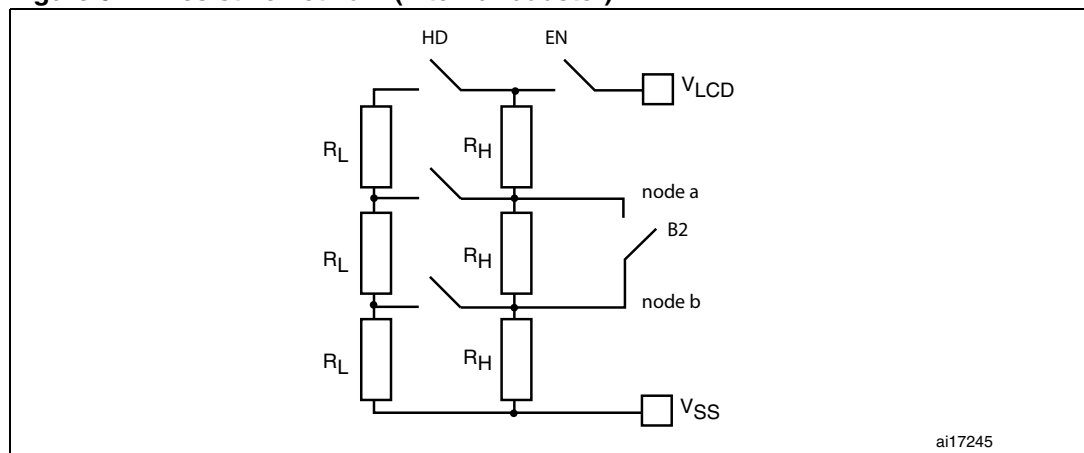
Internal booster

The internal booster is selected by setting VSEL to 40' in LCD_CR2. In this case, the contrast is controlled by adjusting the V_{LCD} by software from 2.6 to 3.3 V in 8 steps.

The internal booster includes two resistive networks which are used to increase the current during transitions and to reduce consumption (see [Figure 9](#)).

- The R_H divider is enabled when the EN signal is set. EN follows the following rules:
 - When LCDEN bit in the LCD_CR3 register is set, the EN signal is '1'
 - When clearing the LCDEN bit in the LCD_CR3, the EN signal is '0' at the end of the even frame in order to avoid a medium voltage level different from 0 during the frame.
- The R_L divider is enabled when the HD signal is set only for a short period of time when the levels of common and segment lines change. This time can be programmed through the Pulse ON bits (PON[2:0]) of the LCD_CR2 register. The HD signal follows the rules described below:
 - If the HD bit and the PON[2:0] bits in the LCD_CR2 are reset, then HD signal is '0'.
 - If the HD bit in the LCD_CR2 register is reset and the PON[2:0] bits in the LCD_CR2 are different from 00 then, the HD signal is '1' during the number of pulses defined in the PON[2:0] bits.
 - If HD bit in the LCD_CR2 register is 1 then HD signal is always 1.

Figure 9. Resistive network (internal booster)



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3.2 Optimizing power consumption

When the LCD controller operates in run mode, decreasing the power consumption results in a lower contrast. As a consequence, the contrast adjustment methods described in [Section 3.1.3](#) can also be used to adjust the power consumption.

When the internal booster is used, the power consumption can be reduced by minimizing the period of time during which the R_L divider is enabled (drive time). However, the drive time to achieve a satisfactory contrast may be longer with a high internal resistance.

However, the STM8L15x microcontroller allows the LCD controller to operate in all low power modes except for Halt mode.

4 Displaying alphanumeric characters on the LCD glass

This section explains how to connect the STM8L15x LCD controller to an LCD glass to display alphanumeric characters. It takes the example of the STM8L1526-EVAL evaluation board using Pacific Display Devices PD-878.

4.1 PD-878 LCD glass

The PD-878 LCD glass mounted on the STM8L1526-EVAL is an eight multiplexed digit display from Pacific Display Devices, the PD-878 (see [Figure 10](#)).

Depending on the type of LCD glass which is used, the user can select the LCD mode by configuring the duty cycle. Each segment terminals can control up four pixels. The integrated LCD controller can control up to 112 segments that can be divided between alphanumeric symbols and several predefined symbols including digit, bell, low-battery symbol, arrows (left, up, right, and down), antenna, and progress bar. Since the LCD glass has in total 128 segments controlled through four COM and 32 segment lines, some of the segments of the LCD glass is not connected in the standard configuration (see [Figure 11](#))

Alphanumeric characters are displayed using 16 segments. [Figure 12](#) shows the segments and reference letters for an alphanumeric character.

Figure 10. Layout for the PD-878

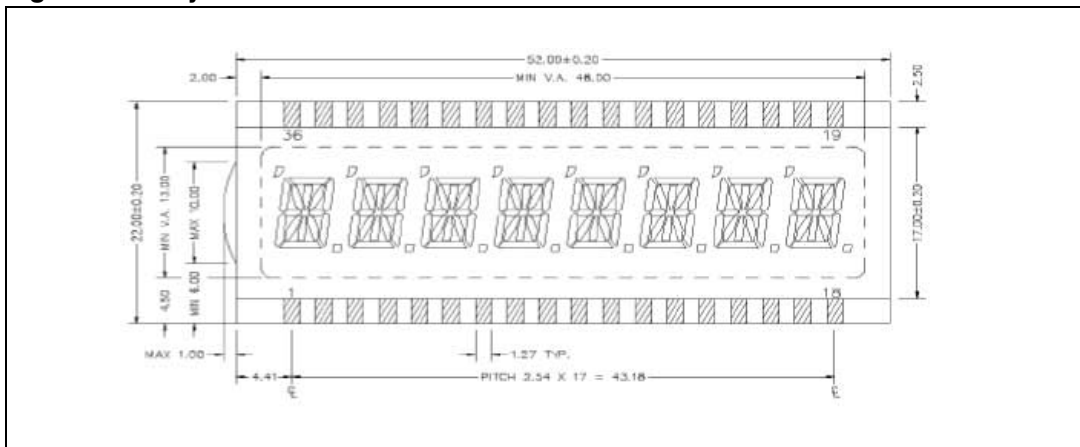


Figure 11. LCD segments used on the STM8L1526-EVAL

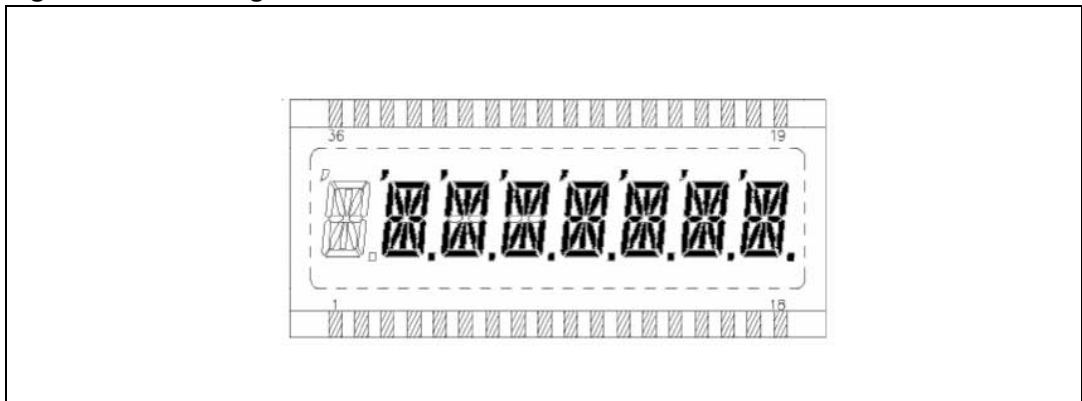
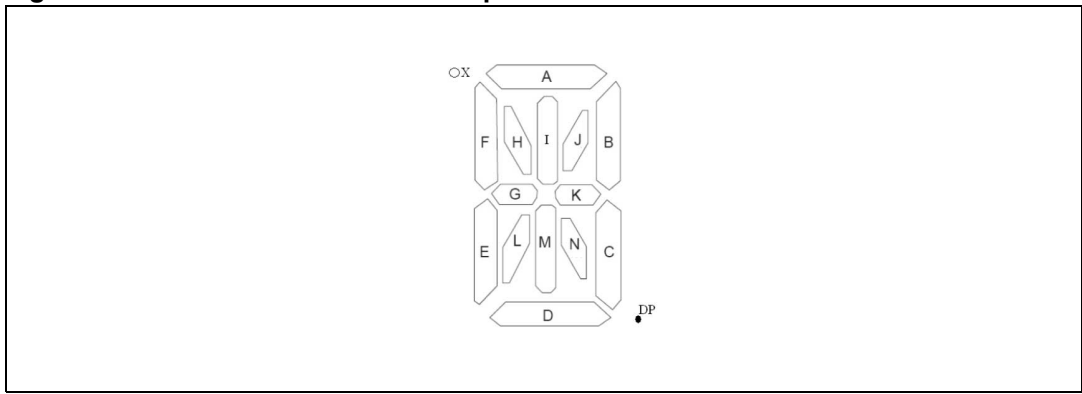


Figure 12. Reference letters for an alphanumeric character on the PD-878



4.2 Connecting the LCD glass to the LCD controller

To display an alphanumeric character on the LCD glass display PD-878, four common lines (COM) and four segment lines (SEG) are required. [Table 1](#) shows the correspondence between the LCD controller segment and the reference letter on the LCD glass.

Table 1. Reference letter for an alphanumeric character on LCD

Couple (COM/SEG)	Segment	Reference letter for an alphanumeric character
COM0/SEG(n)	Segment(n)	X
COM0/SEG(n+1)	Segment(n+1)	I
COM0/SEG(n+2)	Segment(n+2)	A
COM0/SEG(n+3)	Segment(n+3)	H
COM1/SEG(n)	Segment(n+28)	F
COM1/SEG(n+1)	Segment(n+1+28)	J
COM1/SEG(n+2)	Segment(n+2+28)	B
COM1/SEG(n+3)	Segment(n+3+28)	G
COM2/SEG(n)	Segment(n+56)	E

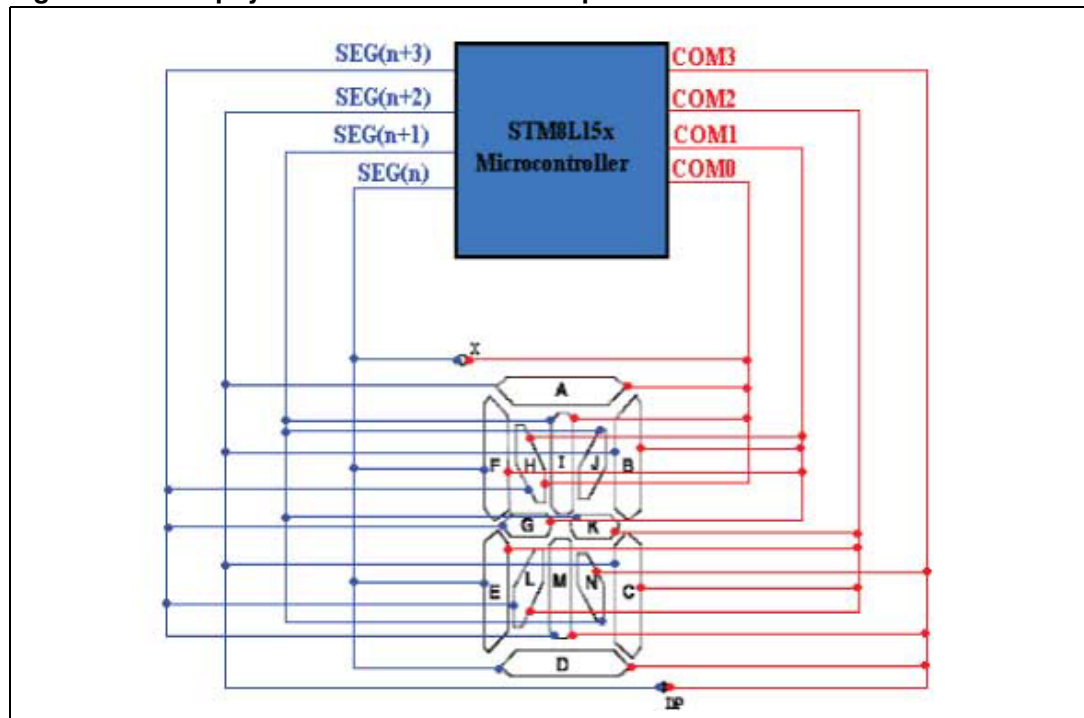
Table 1. Reference letter for an alphanumeric character on LCD (continued)

Couple (COM/SEG)	Segment	Reference letter for an alphanumeric character
COM2/SEG(n+1)	Segment(n+1+56)	K
COM2/SEG(n+2)	Segment(n+2+56)	C
COM2/SEG(n+3)	Segment(n+3+57)	L
COM3/SEG(n)	Segment(n+84)	D
COM3/SEG(n+1)	Segment(n+1+84)	N
COM3/SEG(n+2)	Segment(n+2+84)	DP
COM3/SEG(n+3)	Segment(n+3+84)	M

The LCD segments are individually controlled by setting or clearing the corresponding bit of the LCD Data registers (LCD_RAM[13:0]). The LCD controller module handles the encoding of the physical drive waveforms to the LCD Glass.

The physical connections between each of the 16 segment digits, the segment lines and the common lines must be performed as shown in *Figure 13*.

Figure 13. The physical connection for an alphanumeric character



To be able to make an efficient LCD software driver and optimize LCD character coding in terms of code density, the matrix shown in [Figure 14](#) has been chosen.

Figure 14. Segment driver matrix

	COM0	COM1	COM2	COM3
SEG(n)	{ X ,	F ,	E ,	D }
SEG(n+1)	{ I ,	J ,	K ,	N }
SEG(n+2)	{ A ,	B ,	C ,	DP }
SEG(n+3)	{ H ,	G ,	L ,	M }
n = {0,4,8,12,16,20,24}				

Each matrix element corresponds to one segment on the LCD_RAM[13:0] registers. To deactivate SEG(n) connected to COMi, SEG(n+1),SEG(n+2) and SEG(n+3) must to be inactive when COMi is active. To activate SEG(n), all the other segments must be active when COMi is active. The segment driver controls the segments according to the input segment data coming from the 4 to 1 multiplexers driven by the common driver during each phase.

The following structure provided in the LCD firmware allows to translate alphanumeric characters from ASCII to LCD_RAM[13:0] bits:

```
bit[15:0] = Nibble[3:0] = {LCD_RAM[13:10], LCD_RAM[10:7],
LCD_RAM[6:3], LCD_RAM[3:0]};
```

Bit[15:0] are the 16 matrix terms arranged so that each nibble is related to one LCD_RAM register. The relation between the nibbles and the LCD_RAM registers is conditioned by the LCD digit which is accessed. [Table 2](#) summarizes the correspondence between LCD_RAM register bits (nibble) and LCD character.

Table 2. LCD_RAM bits versus LCD characters

LCD RAM	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCD_RAM0	Character1				Character0			
LCD_RAM1	Character3				Character2			
LCD_RAM2	Character5				Character4			
LCD_RAM3	Character0				Character6			
LCD_RAM4	Character2				Character1			
LCD_RAM5	Character4				Character3			
LCD_RAM6	Character6				Character5			
LCD_RAM7	Character1				Character0			
LCD_RAM8	Character3				Character2			
LCD_RAM9	Character5				Character4			
LCD_RAM10	Character0				Character6			
LCD_RAM11	Character2				Character1			
LCD_RAM12	Character4				Character3			
LCD_RAM13	Character6				Character5			

Displaying a ‘W’ on the LCD glass

The LCD segments B, C, E, F, L, and N must be activated to display the ‘W’ letter (see [Figure 15](#)). These segments must then be transferred from the LCD_RAM registers to the LCD glass. Use the matrix described in [Figure 14](#) to know which bits of the LCD_RAM registers must be set.

The firmware structure provides the value 0x05D2 for Nibble[3:0], corresponding to:

- Nibble[0] = 0x0 = 0000b
- Nibble[1] = 0x5 = 0101b
- Nibble[2] = 0xD = 1101b
- Nibble[3] = 0x2h = 0010b.

To display ‘W’ on position three on the LCD glass, the LCD_RAM registers must be programmed as follows:

- Nibble[0] in the MSB bits for LCD_RAM1 register
- Nibble[1] in the LSB bits for the LCD_RAM5 register
- Nibble[2] in the MSB bits for the LCD_RAM8 register
- Nibble[3] in the LSB bits for the LCD_RAM12 register

Note: All upper case letters and number are converted from ASCII characters to LCD_RAM registers format. The LCD letters and numbers map are stored in two Flash tables (LetterMap and NumberMap) as constants which are used when translating the ASCII characters to LCD RAM registers.

Figure 15. Letter “W” displayed on the PD-878

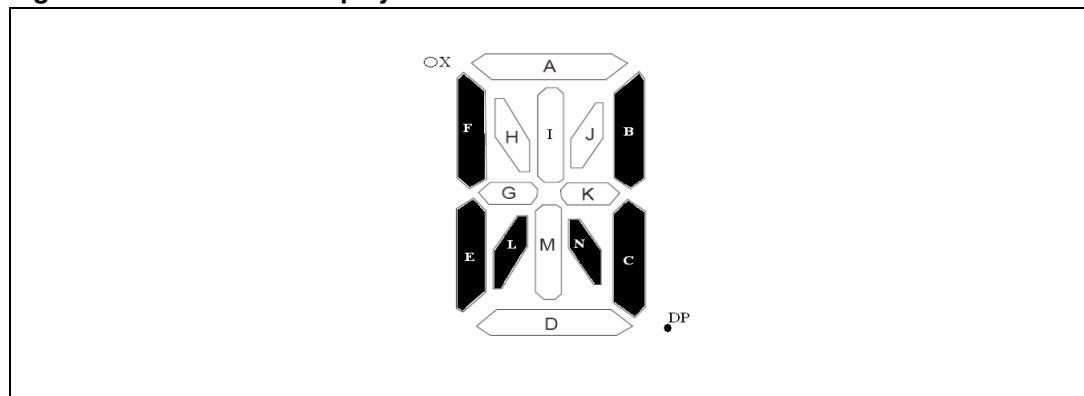


Figure 16. Displaying ‘W’ on the matrix

	COM0	COM1	COM2	COM3
SEG (n)	{ 0 ,	1 ,	1 ,	0 }
SEG (n+1)	{ 0 ,	0 ,	0 ,	1 }
SEG (n+2)	{ 0 ,	1 ,	1 ,	0 }
SEG (n+3)	{ 0 ,	0 ,	1 ,	0 }
	0x 0	5	D	2

5 LCD segment drive firmware

To facilitate the development of customer application, ST provides a firmware to drive the LCD segments.

This firmware runs on the STM8L1526-EVAL evaluation board which provides all the hardware features to interface with an LCD glass. Before executing it, make sure that the MB821 daughter board is connected on the LCD position and that the JP7 jumper on the Key position.

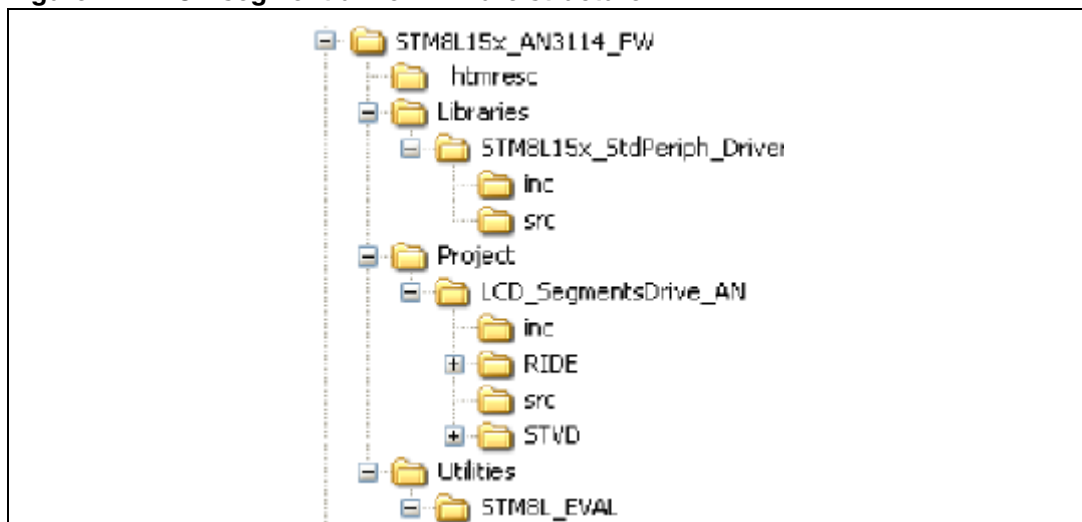
5.1 Firmware package description

The LCD segment drive firmware package contains both the PD-878 LCD glass library and the firmware described in this section.

The firmware package contains the following directories (see [Figure 17](#)):

- **Libraries** directory
- **Project** directory
- **Utilities** directory

Figure 17. LCD segment drive firmware structure



5.1.1 Libraries directory

The **Libraries** directory contains the subdirectories and files that make up the core of the LCD segment drive firmware:

- **inc** subdirectory contains the firmware library header files.
- **src** subdirectory contains the firmware library source files.

5.1.2 Projects directory

The **Projects** directory includes the **LCD_SegmentsDrive_AN** subdirectory which contains the subdirectories and files that make up the core of the LCD glass interface application example:

- **include** subdirectory contains the example header files.
- **source** subdirectory contains the example source files.
- **project** subdirectory contains the projects used to compile the firmware files.

5.1.3 Utilities directory

The **Utilities** directory contains the subdirectories and files used to control the STM8L1526-EVAL board hardware, except for the MCU.

5.2 Firmware description

The STM8L15x features a real-time clock (RTC) which provides a set of continuously running counters that can be used to implement a clock-calendar function. The counters values can be written to set the current time of the system. After the evaluation board is powered up, the default time (00:00:00) is displayed on the LCD glass and the first digit of the hour field can be changed.

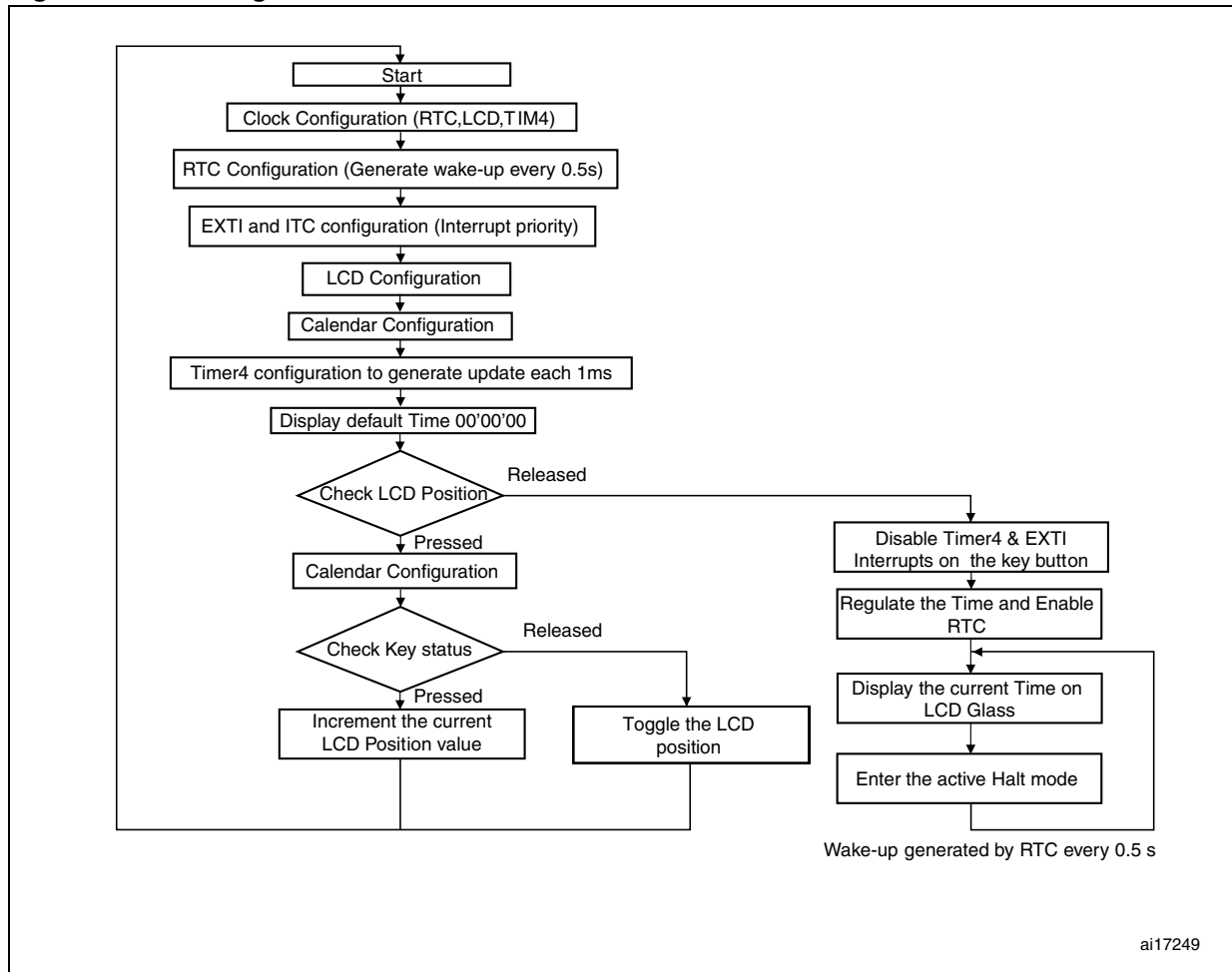
To set the time:

1. Press the **Key** button to increment the active digit. When the **Key** button is released the selected value is stored and the next digit can be changed. The digit allowed values depend on the corresponding field (hour, minute or seconds).
2. Repeat these two steps for the six digits.

Once all the digits are set, the RTC calendar registers are configured, and the current time is displayed on the LCD. The application enters Active-halt mode and is woken up by the RTC wakeup interrupt to display the current time. It then goes back to the Active-halt mode. This operation is repeated infinitely.

Note: Time setting is made only once after the application startup. The application must be restarted to modify the time.

Figure 18. LCD segment drive software flowchart



5.2.1 LCD controller setup

The following steps are recommended to configure the LCD controller:

1. Enable the LCD clock
2. Configure the RTC clock source
3. Configure the frequency obtain the required frame frequency in the operating frequency range of the PD-878 LCD glass, that is between 30 and 85 HZ.

In this application the STM8L15x LCD controller is configured as follows:

- LCD clock source frequency
 $f_{CLK} = \text{LSE frequency} = 32.768 \text{ KHz}$
- Prescaler factor = 2
- Divider factor = 18 (16 + 2)
- Mode = 1/4 Duty, 1/3 Bias
- LCD clock frequency

The LCD clock frequency, f_{LCD} , is given by the equation below:

$$f_{LCD} = (f_{CLK} \times \text{Duty}) / (\text{Prescaler} \times \text{Divider})$$

As a result, f_{LCD} equals 228 Hz, and f_{frame} 57 Hz.

6 Conclusion

The LCD segment drive firmware allows to develop an LCD glass based application with the minimum firmware and hardware resources.

7 Revision history

Table 3. Document revision history

Date	Revision	Changes
22-Jan-2010	1	Initial release.

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